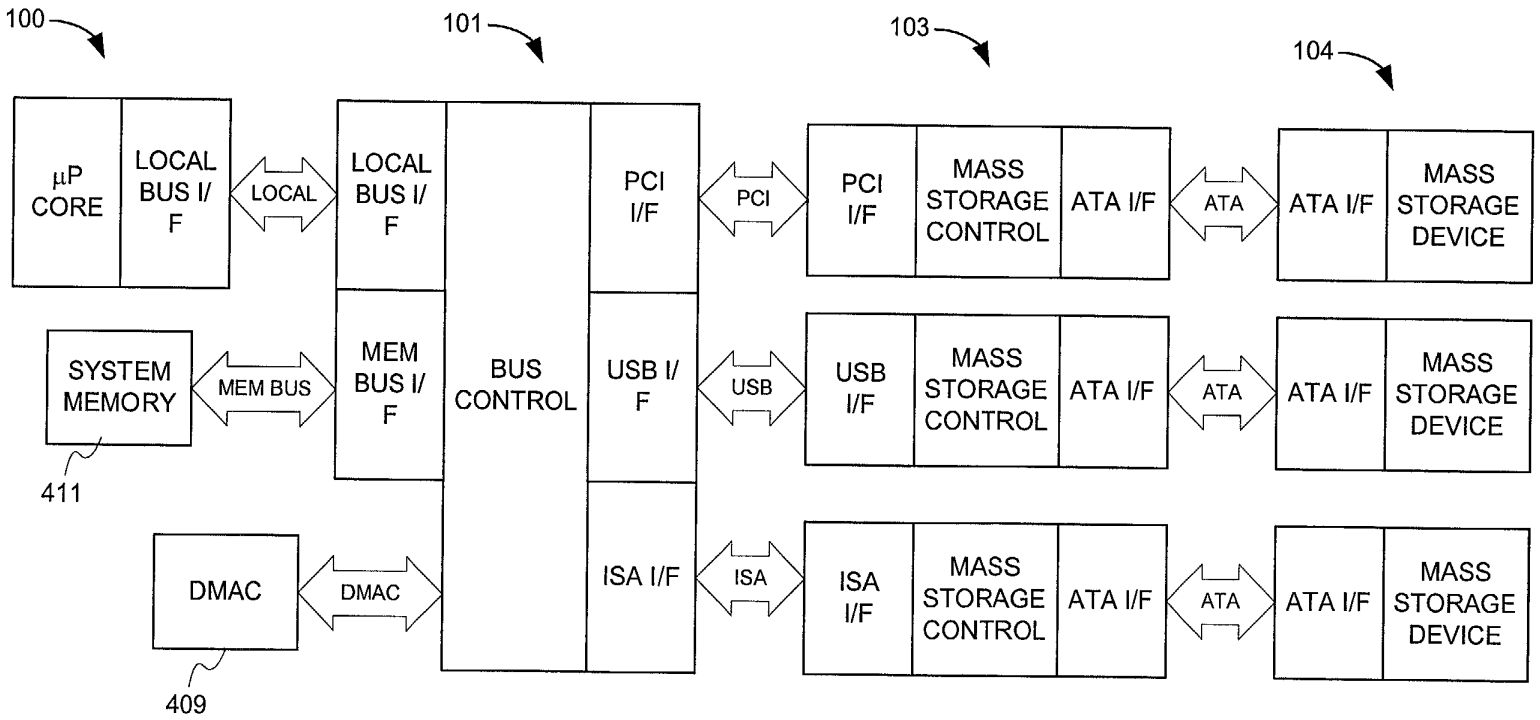

FIG. 1
(Prior Art)

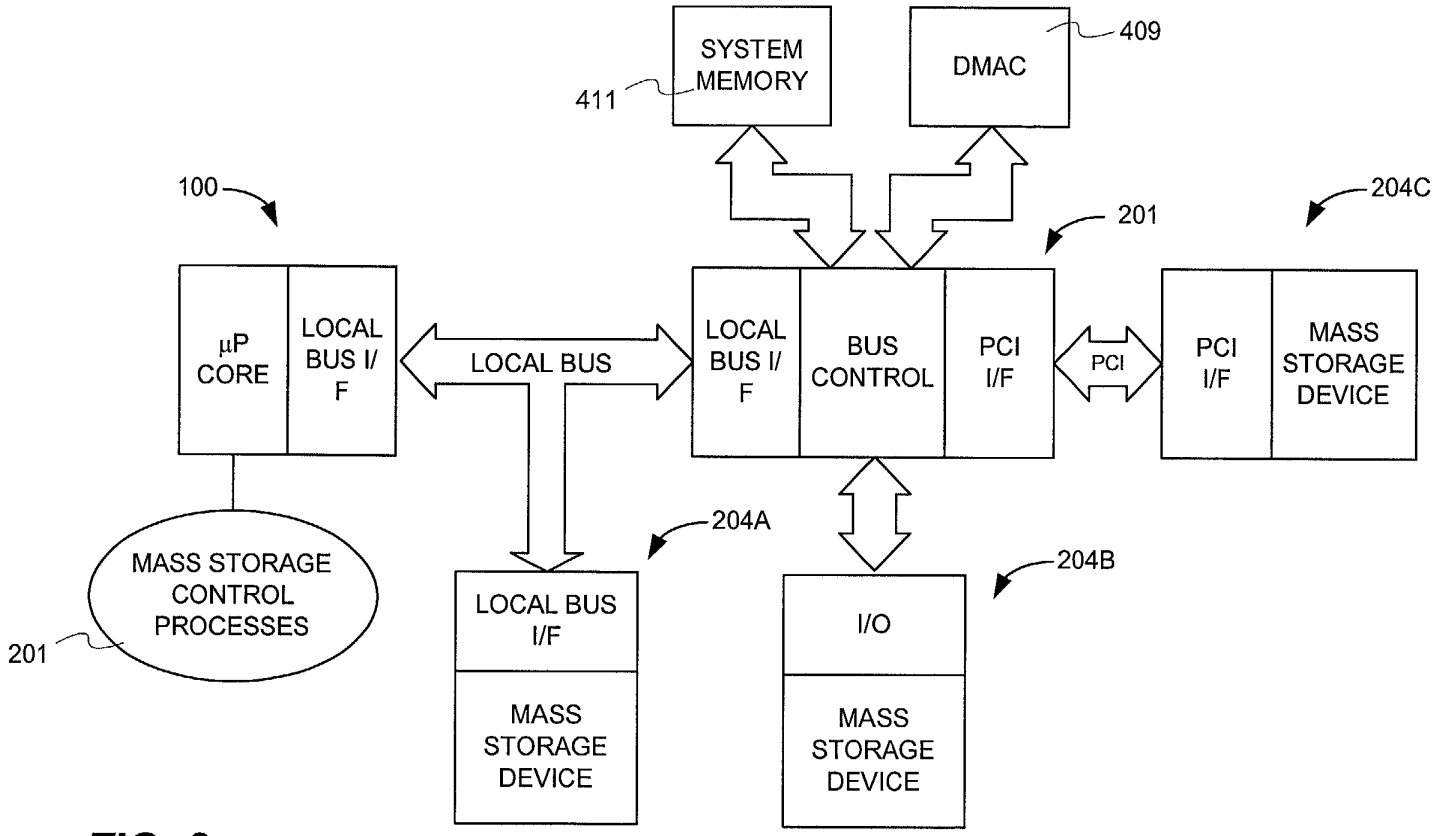
SYSTEM MEMORY
411
DMAC
409
100
201
204C
μP CORE
LOCAL BUS I/F
LOCAL BUS
LOCAL BUS I/F
BUS CONTROL
PCI I/F
PCI
PCI I/F
MASS STORAGE DEVICE
MASS STORAGE CONTROL PROCESSES
201
204A
LOCAL BUS I/F
MASS STORAGE DEVICE
204B
I/O
MASS STORAGE DEVICE

FIG. 2

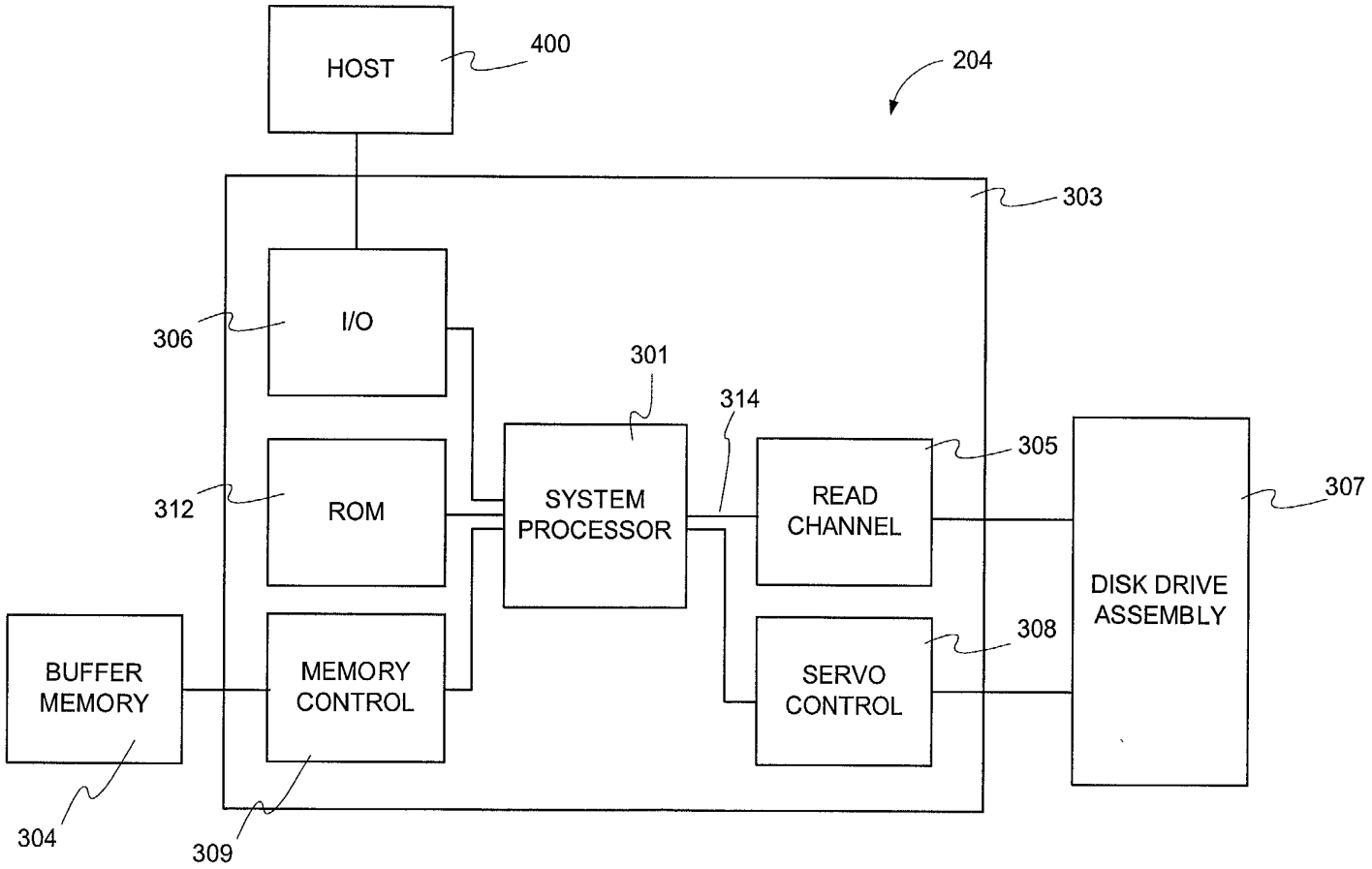
HOST
400
204
303
I/O
306
301
314
ROM
312
SYSTEM PROCESSOR
READ CHANNEL
305
307
DISK DRIVE ASSEMBLY
BUFFER MEMORY
MEMORY CONTROL
SERVO CONTROL
308
304
309

FIG. 3

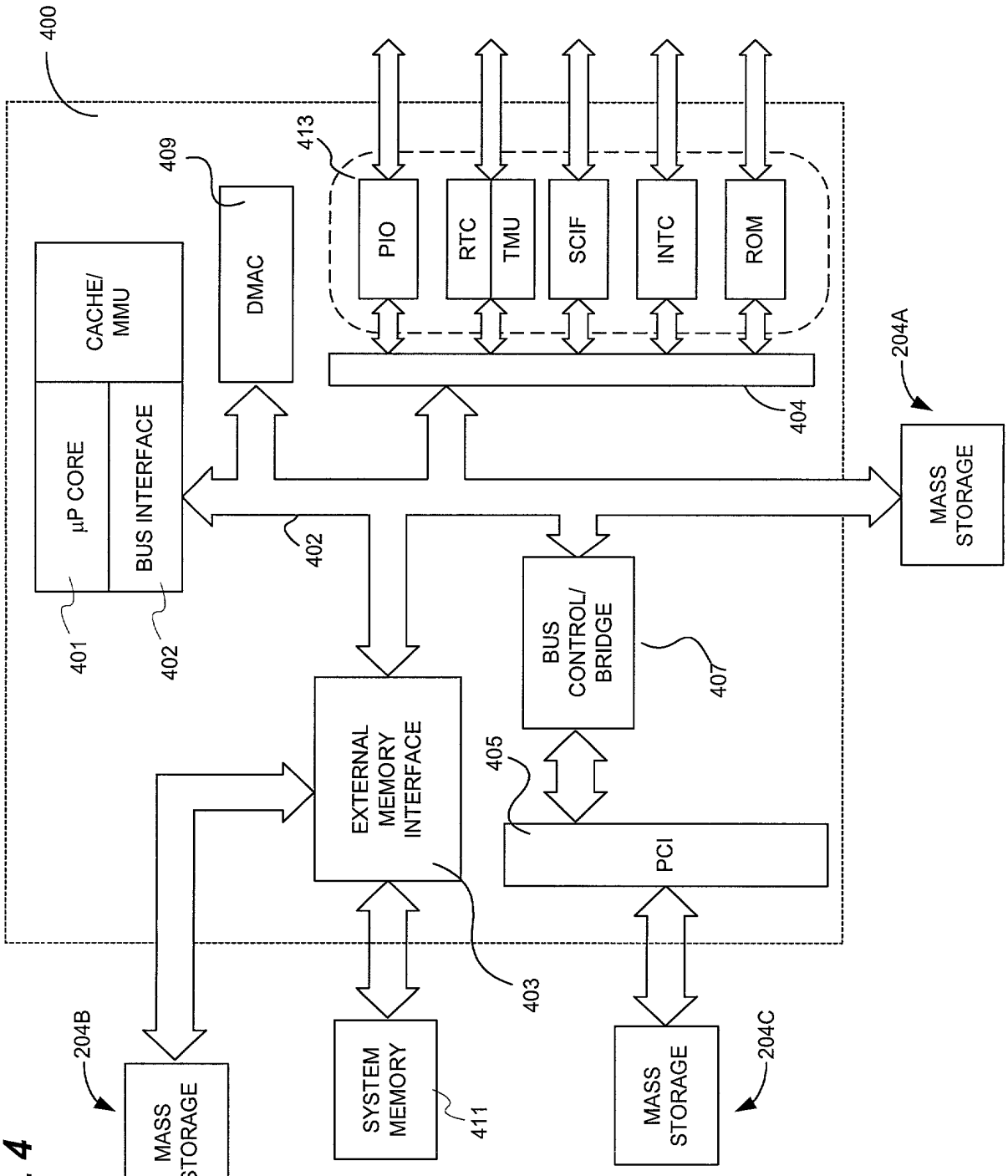
400
409
413
DMAC
PIO
RTC
TMU
SCIF
INTC
ROM
CACHE/
MMU
µP CORE
BUS INTERFACE
404
204A
MASS
STORAGE
401
402
402
BUS
CONTROL/
BRIDGE
407
EXTERNAL
MEMORY
INTERFACE
405
PCI
403
204B
MASS
STORAGE
SYSTEM
MEMORY
411
MASS
STORAGE
204C

FIG. 4

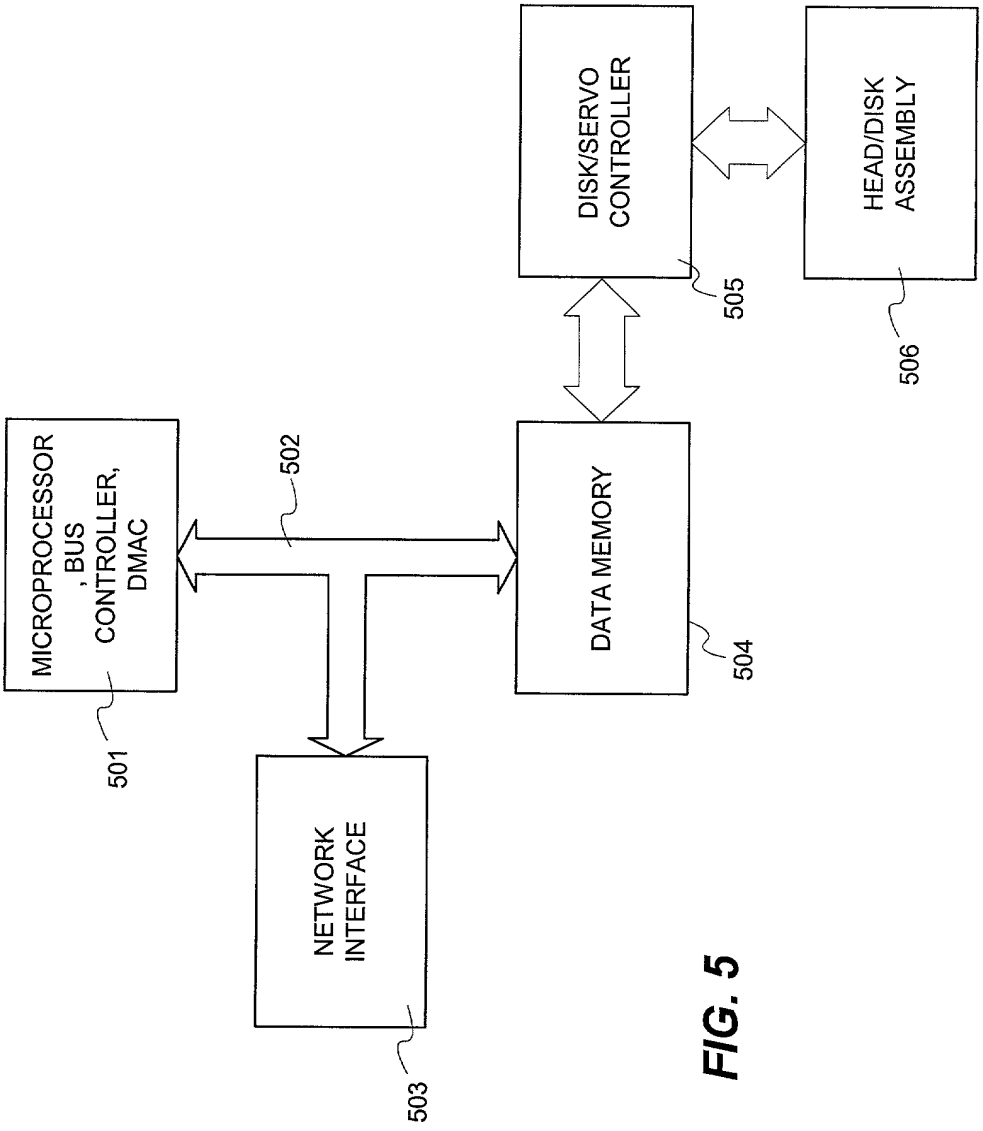
MICROPROCESSOR , BUS CONTROLLER, DMAC
501
502
NETWORK INTERFACE
503
DATA MEMORY
504
DISK/SERVO CONTROLLER
505
HEAD/DISK ASSEMBLY
506

FIG. 5

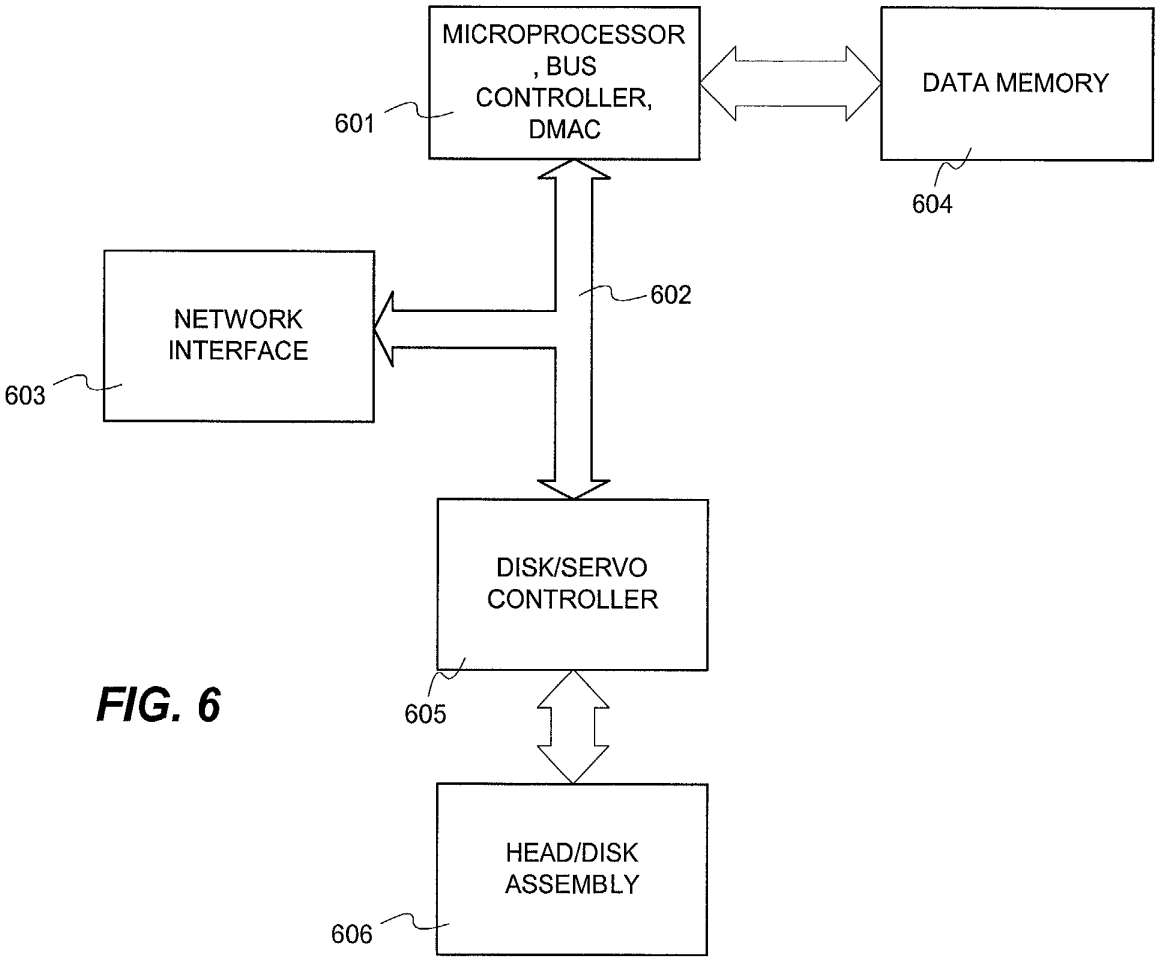
MICROPROCESSOR , BUS CONTROLLER, DMAC
601
DATA MEMORY
604
602
NETWORK INTERFACE
603
DISK/SERVO CONTROLLER
605
HEAD/DISK ASSEMBLY
606

FIG. 6

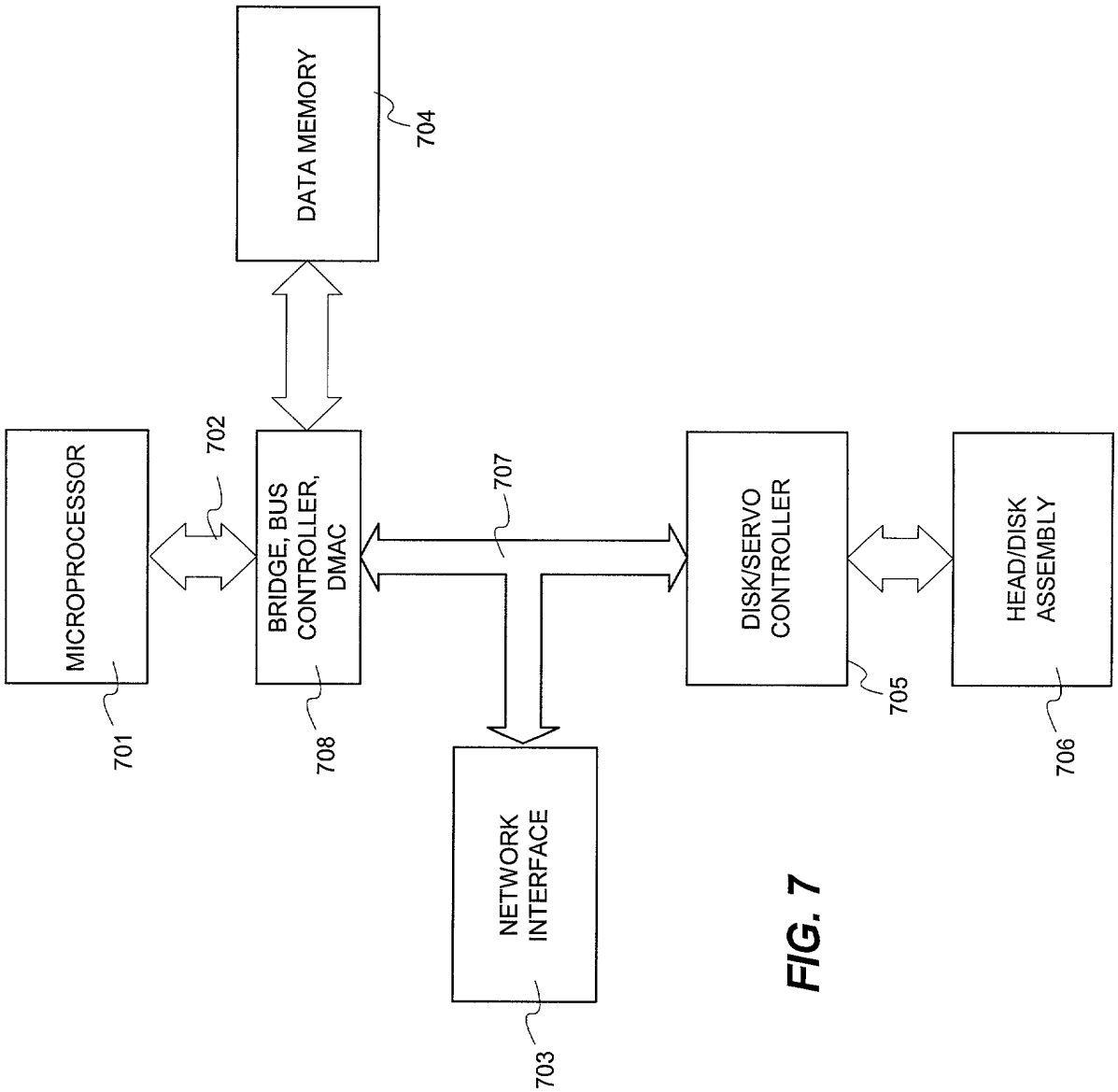
DATA MEMORY
704
MICROPROCESSOR
701
702
BRIDGE, BUS CONTROLLER, DMAC
708
707
DISK/SERVO CONTROLLER
705
HEAD/DISK ASSEMBLY
706
NETWORK INTERFACE
703

FIG. 7